



# STD40NE03L

## N - CHANNEL 30V - 0.012 Ω - 40A TO-252 STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD40NE03L	30 V	< 0.016 Ω	40 A

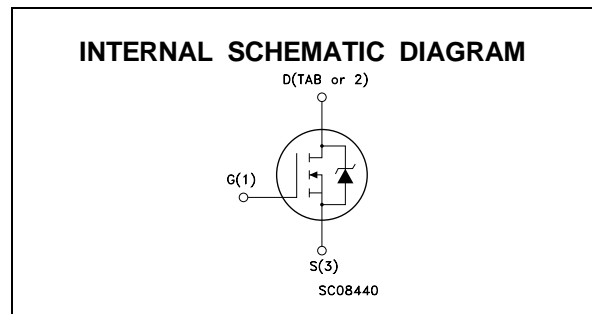
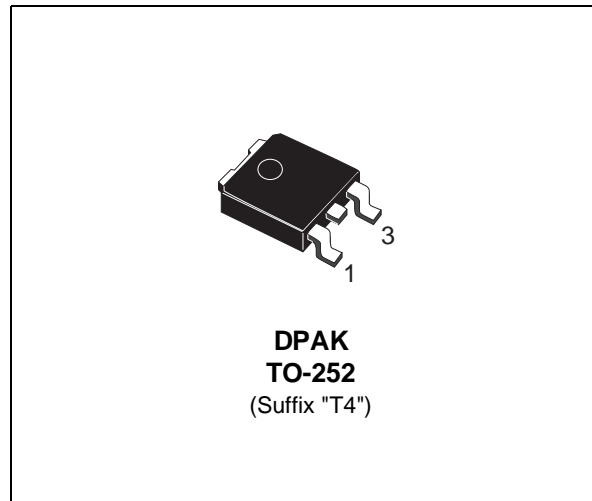
- TYPICAL R<sub>DS(on)</sub> = 0.012 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- APPLICATION ORIENTED CHARACTERIZATION
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate-source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	20**	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	20**	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	160	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	55	W
	Derating Factor	0.37	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(\*\*) Value limited only by the package

(1) I<sub>SD</sub> ≤ 20A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

## STD40NE03L

### THERMAL DATA

R <sub>thj-pcb</sub>	Thermal Resistance Junction-PC Board	Max	2.7	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	100	°C/W
R <sub>thj-sink</sub>	Thermal Resistance Case-sink	Typ	1.5	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		275	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 15 V)	100	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>c</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1	1.7	2.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 20 A V <sub>GS</sub> = 5 V I <sub>D</sub> = 20 A		0.012	0.016 0.022	Ω Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> V <sub>GS</sub> = 10 V	40			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> I <sub>D</sub> = 20 A	15	28		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0 V		2200		pF
C <sub>oss</sub>	Output Capacitance			570		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			200		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, see fig. 3)		38		ns
$t_r$	Rise Time			260		ns
$Q_g$	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 64\text{ A}$ $V_{GS} = 5\text{ V}$		35	45	nC
$Q_{gs}$	Gate-Source Charge			18		nC
$Q_{gd}$	Gate-Drain Charge			13		nC

**SWITCHING OFF**

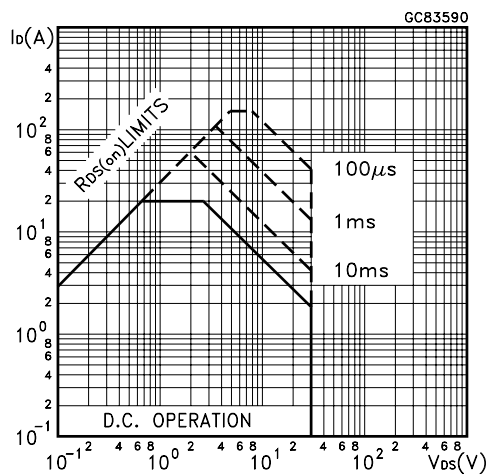
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, see fig. 3)		75		ns
$t_f$	Fall Time			50		ns
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 24\text{ V}$ $I_D = 64\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Inductive Load, see fig. 5)		35		ns
$t_f$	Fall Time			120		ns
$t_c$	Cross-over Time			175		ns

**SOURCE DRAIN DIODE**

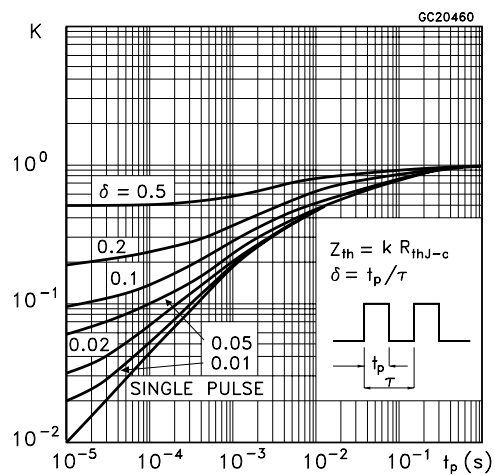
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				40	A
$I_{SDM(\bullet)}$	Source-drain Current (pulsed)				160	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 40\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 64\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		55		ns
$Q_{rr}$	Reverse Recovery Charge			0.1		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			3.5		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %  
 (•) Pulse width limited by safe operating area

**Safe Operating Area**

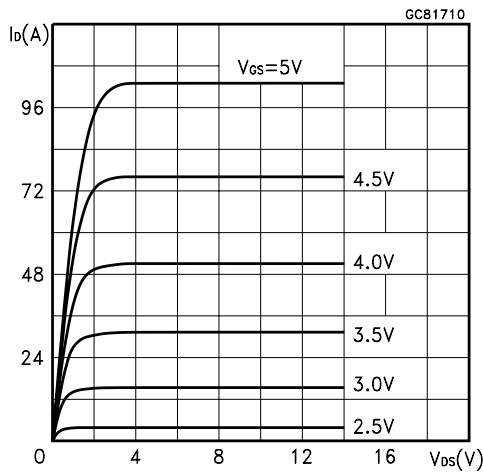


**Thermal Impedance**

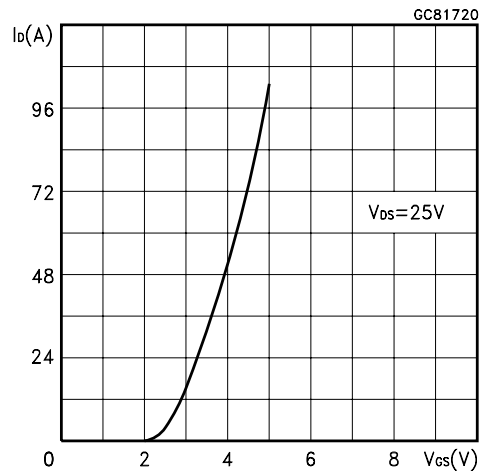


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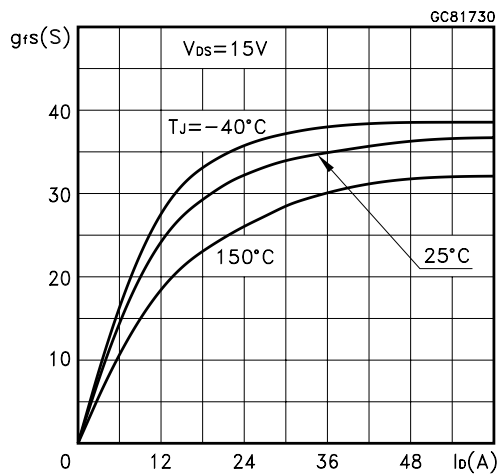
## Output Characteristics



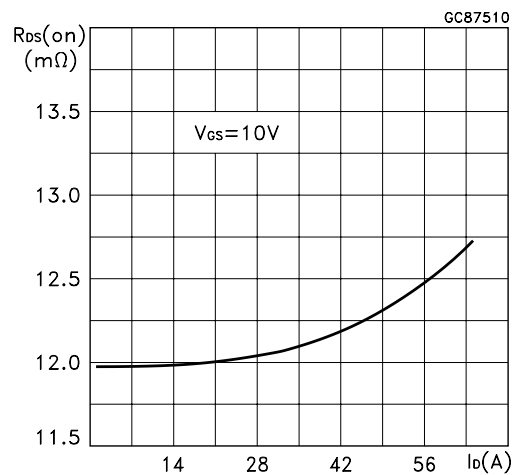
## Transfer Characteristics



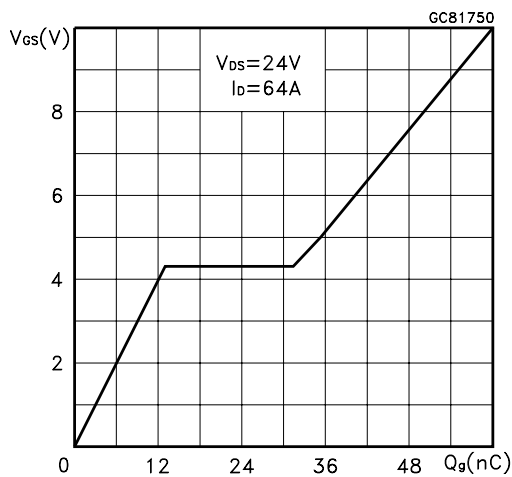
## Transconductance



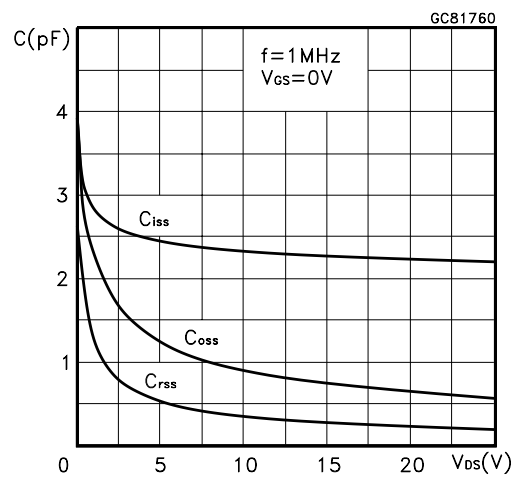
## Static Drain-source On Resistance



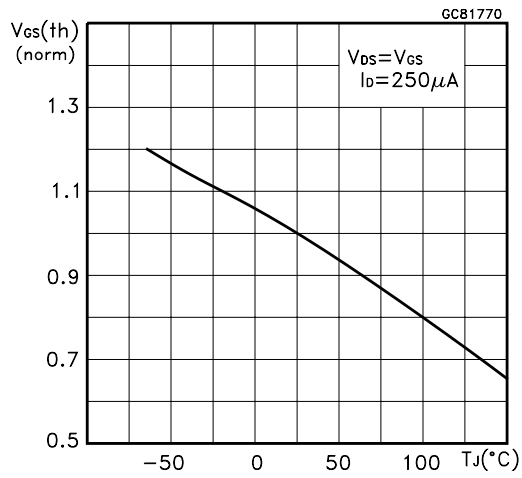
## Gate Charge vs Gate-source Voltage



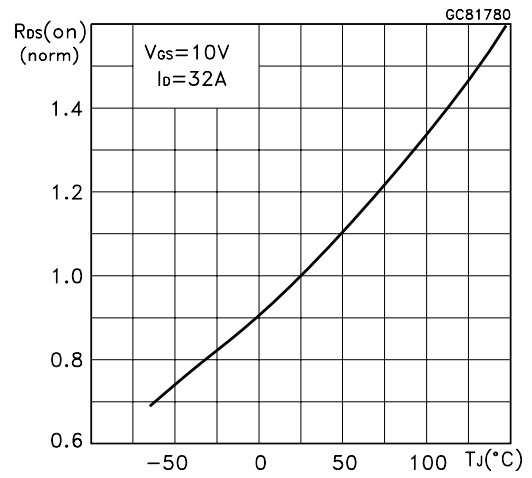
## Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

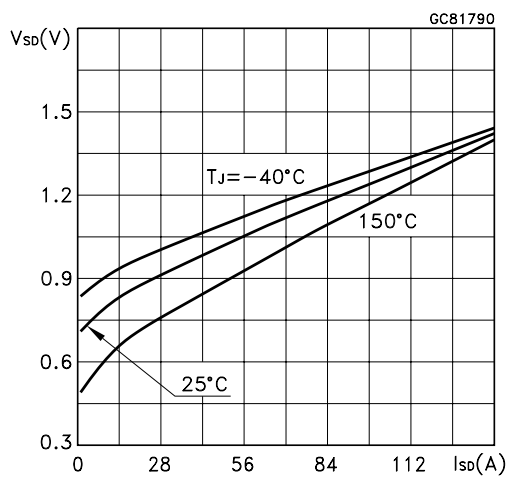


Fig. 1: Unclamped Inductive Load Test Circuit

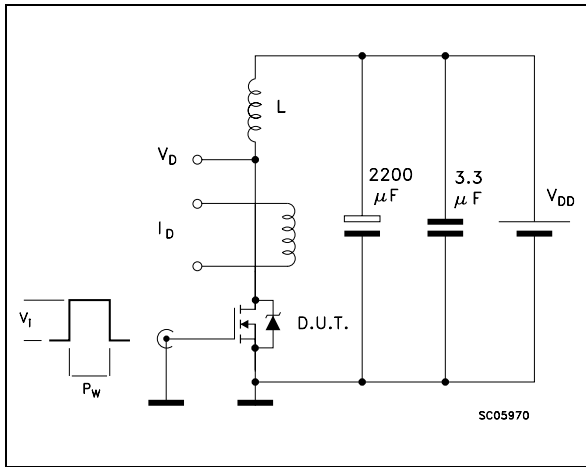


Fig. 2: Unclamped Inductive Waveform

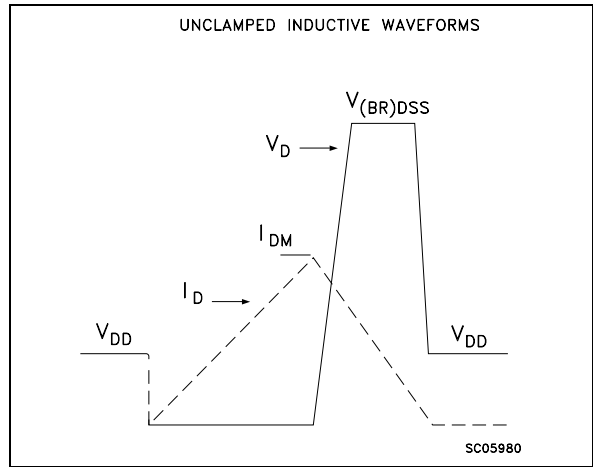


Fig. 3: Switching Times Test Circuits For Resistive Load

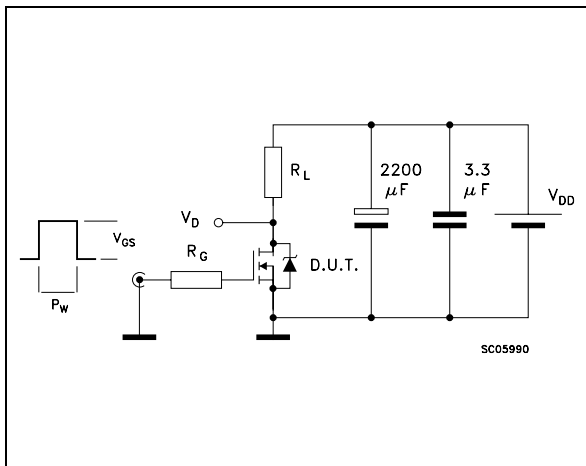


Fig. 4: Gate Charge test Circuit

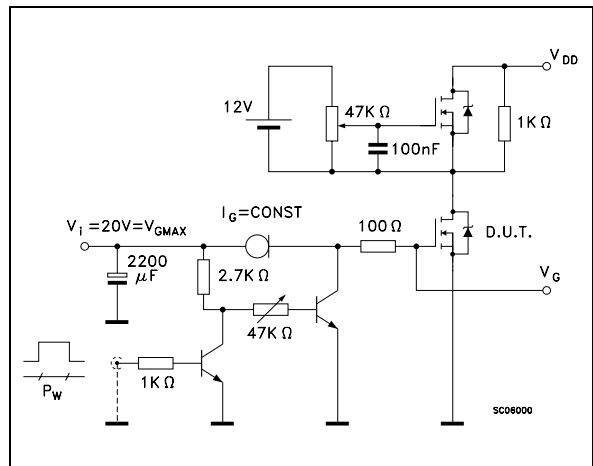
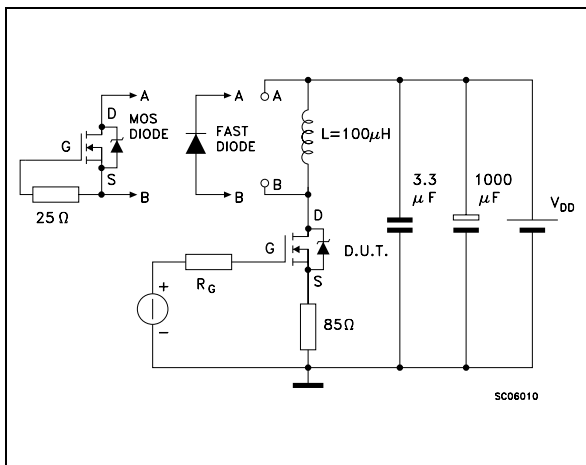
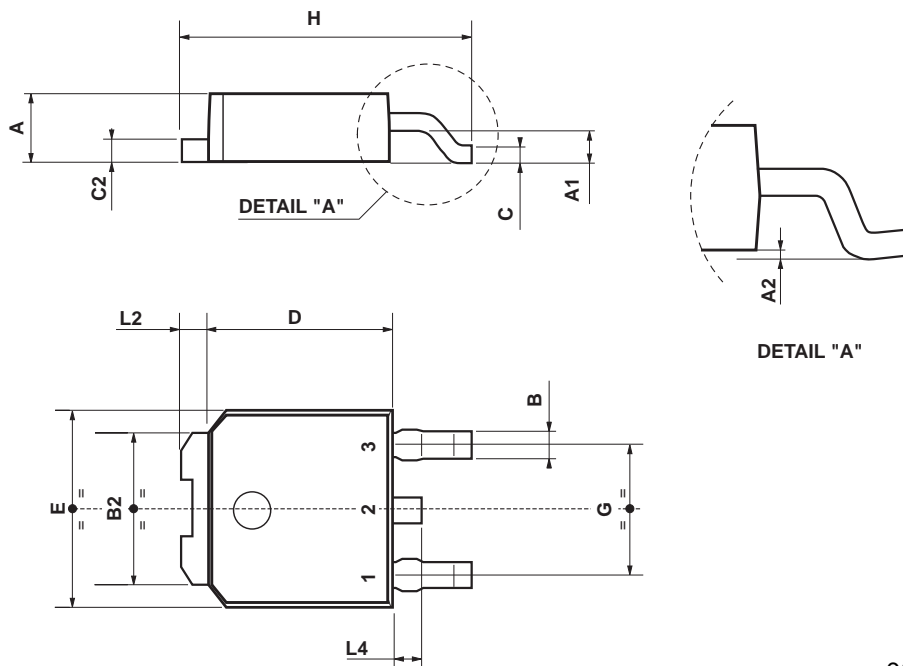


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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